Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1 to 15. (Canceled).

16. (New) A data processing arrangement, comprising:

at least one standard processor configured to process data in a sequential manner;

an instruction pipeline including a FIFO; and

a reconfigurable array adapted for processing data, the reconfigurable array comprising a plurality of processing cells;

wherein:

the instruction pipeline is arranged for coupling the at least one standard processor to the reconfigurable array;

the reconfigurable array is coupled to the instruction pipeline such that at least one of configuration load instructions and configuration preload instructions are transferable to at least one of the array and a configuration manager coupled thereto; and

said FIFO is arranged for storing at least some of the at least one of configuration load instructions and configuration preload instructions in a manner that makes them available to be fed from the FIFO to the reconfigurable array, the feeding effecting at least one of loading and preloading of configuration data, the configuration data defining how data processing is to proceed.

17. (New) The data processing arrangement of claim 16, wherein said FIFO is arranged for storing only the at least some of the configuration load instructions.

18. (New) The data processing arrangement of claim 17, wherein the at least some of the configuration load instructions includes all of the configuration load instructions.

19. (New) The data processing arrangement of claim 16, wherein said FIFO is arranged for storing only the at least some of the configuration preload instructions.

20. (New) The data processing arrangement of claim 19, wherein the at least some of the configuration preload instructions includes all of the configuration preload instructions.

21. (New) The data processing arrangement of claim 16, wherein said FIFO is arranged for storing at least some of the configuration load instructions and at least some of the configuration preload instructions.

22. (New) The data processing arrangement of claim 21, wherein the at least some of the configuration load instructions includes all of the configuration load instructions and the at least some of the configuration preload instructions includes all of the configuration preload instructions.

23. (New) The data processing arrangement of any of claims 16 to 22, wherein the instruction pipeline is coupled to the reconfigurable array such that configuration load instructions from the instruction pipeline are transferable to the array only.

24. (New) The data processing arrangement of any of claims 16 to 22, wherein the instruction pipeline is coupled to the reconfigurable array such that configuration load instructions from the instruction pipeline are transferable to the configuration manager only.

25. (New) The data processing arrangement of any of claims 16 to 22, wherein the instruction pipeline is coupled to the reconfigurable array such that configuration load instructions from the instruction pipeline are transferable to both the array and the configuration manger.

26. (New) The data processing arrangement of any of claim 16 to 22, wherein the array is coupled to exactly one standard processor adapted for processing data in a sequential manner.

27. (New) The data processing arrangement of claim 16, wherein the plurality of processing cells are coarse-grained cells.

28. (New) The data processing arrangement of claim 17, wherein the plurality of processing cells are coarse-grained cells.

29. (New) The data processing arrangement of claim 28, wherein the at least some of the configuration load instructions includes all of the configuration load instructions.

30. (New) The data processing arrangement of claim 19, wherein the plurality of processing cells are coarse-grained cells.

31. (New) The data processing arrangement of claim 30, wherein the at least some of the configuration preload instructions includes all of the configuration preload instructions.

32. (New) The data processing arrangement of claim 21, wherein the plurality of processing cells are coarse-grained cells.

33. (New) The data processing arrangement of claim 32, wherein the at least some of the configuration load instructions includes all of the configuration load instructions and the at least some of the configuration preload instructions includes all of the configuration preload instructions.

34. (New) The data processing arrangement of any of claims 16-22 and 27-33, wherein the plurality of processing cells are reconfigurable at runtime.

35. (New) The data processing arrangement of any of claims 16-22 and 27-33, wherein the reconfigurable array is an FPGA.

36. (New) The data processing arrangement of any of claims 16-22 and 27-33, wherein the reconfigurable array is a DSP.

37. (New) The data processing arrangement of any of claims 16-22 and 27-33, wherein the reconfigurable array is a data-flow-processor.

38. (New) The data processing arrangement of any of claims 16-22 and 27-33, wherein the plurality of processing cells are reconfigurable at runtime without disturbing data processing by other cells.

39. (New) The data processing arrangement of claim 38, wherein the reconfigurable array supports pipeline stages of Load, Execute, and Store.

40. (New) The data processing arrangement of any of claims 16-22 and 27-33, wherein configurations executed on the reconfigurable array are non-preemptive.

41. (New) The data processing arrangement of any of claims 16-22 and 27-33, wherein:

the plurality of processing cells are reconfigurable at runtime without disturbing data processing by other cells; and

configurations executed on the reconfigurable array are non-preemptive.

42. (New) A data processing method, comprising:

providing at least one standard processor for processing data in a sequential manner; and

providing an instruction pipeline that pipelines instructions and couples a reconfigurable array to the at least one standard processor as a virtual processor in a Simultaneous Multithreading (SMT) environment, the reconfigurable array including a plurality of data processing cells.

43. (New) The data processing method of claim 42, wherein the plurality of processing cells are coarse-grained cells.

44. (New) The data processing method of either of claims 42 and 43, wherein the reconfigurable array is runtime reconfigurable.

45. (New) The data processing method of claim 42, wherein the reconfigurable array is an FPGA.

46. (New) The data processing method of claim 42, wherein the reconfigurable array is a DSP.

47. (New) The data processing method of claim 42, wherein the reconfigurable array is a data-flow-processor.

48. (New) The data processing method of either of claims 42 and 43, wherein configurations executed on the reconfigurable array are non-preemptive.

49. (New) The data processing method of claim 42, wherein the instruction pipeline includes a FIFO and the reconfigurable array is coupled to the instruction pipeline such that at least one of configuration load instructions and configuration preload instructions are transferable to at least one of the array and a configuration manager coupled thereto, the method further comprising:

storing, by the FIFO, at least some of the at least one of configuration load instructions and configuration preload instructions in a manner that makes them available to be fed from the FIFO to the reconfigurable array, the feeding effecting at least one of loading and preloading of configuration data, the configuration data defining how data processing is to proceed.

50. (New) The data processing method of claim 49, wherein said FIFO is arranged for storing only the at least some of the configuration load instructions.

51. (New) The data processing method of claim 50, wherein the at least some of the configuration load instructions includes all of the configuration load instructions.

52. (New) The data processing method of claim 49, wherein said FIFO is arranged for storing only the at least some of the configuration preload instruction.

53. (New) The data processing method of claim 52, wherein the at least some of the configuration preload instructions includes all of the configuration preload instructions.

54. (New) The data processing method of claim 49, wherein said FIFO is arranged for storing at least some of the configuration load instructions and at least some of the configuration preload instructions.

55. (New) The data processing method of claim 54, wherein the at least some of the configuration load instructions includes all of the configuration load instructions and the at least some of the configuration preload instructions includes all of the configuration preload instructions.

56. (New) The data processing method of claim 49, further comprising:

replicating at least some preload-FIFO for each virtual processor instance.

57. (New) A data processing method, comprising:

providing a reconfigurable array of data processing cells for data processing;

providing at least one standard processor for processing data in a sequential manner, the at least one standard processor including an instruction pipeline via which the reconfigurable array is coupled to the at least one standard processor; and

coupling the reconfigurable array to a memory hierarchy via an explicitly software managed cache.

58. (New) The data processing method of claim 57, wherein the plurality of processing cells are coarse-grained cells.

59. (New) The data processing method of either of claims 57 and 58, wherein the reconfigurable array is runtime reconfigurable.

60. (New) The data processing method of claim 57, wherein the reconfigurable array is an FPGA.

61. (New) The data processing method of claim 57, wherein the reconfigurable array is a DSP.

62. (New) The data processing method of claim 57, wherein the reconfigurable array is a data-flow-processor.

63. (New) The data processing method of either of claims 57 and 58, wherein configurations executed on the reconfigurable array are non-preemptive.

64. (New) The data processing method of claim 57, wherein the explicitly software managed cache is preloadable via a configuration configured onto the reconfigurable array.

65. (New) The data processing method of claim 57, wherein the explicitly software managed cache is preloadable via a burst-preload instruction triggered by the at least one standard processor.

66. (New) The data processing method of claim 57, wherein the at least one standard processor is a RISC processor.

67. (New) The data processing method of claim 57, wherein the explicitly software managed cache is written back to the memory via a synchronization instruction.

68. (New) The data processing method of claim 57, wherein the instruction pipeline includes a FIFO and the reconfigurable array is coupled to the instruction pipeline such that at least one of configuration load instructions and configuration preload instructions are transferable to at least one of the array and a configuration manager coupled thereto, the method further comprising:

storing, by the FIFO, at least some of the at least one of configuration load instructions and configuration preload instructions in a manner that makes them available to be fed from the FIFO to the reconfigurable array, the feeding effecting at least one of loading and preloading of configuration data, the configuration data defining how data processing is to proceed.

69. (New) The data processing method of claim 68, wherein said FIFO is arranged for storing only the at least some of the configuration load instructions.

70. (New) The data processing method of claim 69, wherein the at least some of the configuration load instructions includes all of the configuration load instructions.

71. (New) The data processing method of claim 68, wherein said FIFO is arranged for storing only the at least some of the configuration preload instruction.

72. (New) The data processing method of claim 71, wherein the at least some of the configuration preload instructions includes all of the configuration preload instructions.

73. (New) The data processing method of claim 68, wherein said FIFO is arranged for storing at least some of the configuration load instructions and at least some of the configuration preload instructions.

74. (New) The data processing method of claim 73, wherein the at least some of the configuration load instructions includes all of the configuration load instructions and the at least some of the configuration preload instructions includes all of the configuration preload instructions.

75. (New) A data processing arrangement, comprising:

at least one standard processor adapted for processing data in a sequential manner, the at least one standard processor including an instruction pipeline;

a reconfigurable array including a plurality of data processing cells coupled to the at least one standard processor via the instruction pipeline; and

a plurality of IRAM memory elements coupled to the reconfigurable array, at least some of the IRAM memory elements adapted for storing local cache copies of a main memory.

76. (New) The data processing arrangement of claim 75, wherein at least some of the IRAM memory elements include multiple IRAM instances.

77. (New) The data processing arrangement of claim 76, wherein at least some of the IRAM memory elements are associated with at least one of a starting address, state information, and an address TAG.

78. (New) The data processing arrangement of claim 77, wherein the at least some of the IRAM memory elements are associated with the starting address.

79. (New) The data processing arrangement of claim 77, wherein the at least some of the IRAM memory elements are associated with the state information.

80. (New) The data processing arrangement of claim 77, wherein the at least some of the IRAM memory elements are associated with the address TAG.

81. (New) The data processing arrangement of claim 80, wherein, if no address TAG matches a data access, a corresponding memory area is newly loaded into an empty IRAM instance.

82. (New) The data processing arrangement of claim 81, wherein, if no empty IRAM instance is available, an unmodified instance is declared empty and overwritten with the newly loaded memory area.

83. (New) The data processing arrangement of claim 81, wherein, if no empty IRAM instance is available, a modified instance is cleaned by writing back its data to the main memory.

84. (New) The data processing arrangement of claim 83, wherein a state machine cleans unused IRAM instances by writing back their content in unused memory cycles.

85. (New) The data processing arrangement of claim 77, wherein the at least some of the IRAM memory elements are associated with the starting address and the state information.

86. (New) The data processing arrangement of claim 77, wherein the at least some of the IRAM memory elements are associated with the starting address and the address TAG.

87. (New) The data processing arrangement of claim 77, wherein the at least some of the IRAM memory elements are associated with the starting address, state information, and address TAG.

88. (New) The data processing arrangement of claim 77, wherein the at least some of the IRAM memory elements are associated with the state information and the address TAG.

89. (New) The data processing arrangement of any of claims 75 to 88, wherein the plurality of data processing cells are coarse-grained.

90. (New) The data processing arrangement of claim 89, wherein the reconfigurable array is runtime reconfigurable.

91. (New) The data processing arrangement of claim 90, wherein the reconfigurable array is one of an FPGA, a DSP, and a data-flow-processor.

92. (New) A data processing method, comprising:

providing a reconfigurable array of data processing cells for data processing;

providing at least one standard processor for processing data in a sequential manner, the at least one standard processor including an instruction pipeline via which the reconfigurable array is coupled to the at least one standard processor; and

coupling the reconfigurable array to a cache, which is explicitly software managed to contain local cache copies of a main memory, the cache including a plurality of IRAM memory elements.

93. (New) The data processing method of claim 92, wherein the data processing cells are coarse-grained cells.

94. (New) The data processing method of claim 93, wherein the reconfigurable array is runtime reconfigurable.

95. (New) The data processing method of any of claims 92-94, wherein the reconfigurable array is an FPGA.

96. (New) The data processing method of any of claims 92-94, wherein the reconfigurable array is a DSP.

97. (New) The data processing method any of claims 92-94, wherein the reconfigurable array is a data-flow-processor.

98. (New) The data processing method of claim 92, wherein configurations executed on the reconfigurable array are non-preemptive.

99. (New) The data processing method of claim 92, wherein the explicitly software managed cache is preloadable via a configuration configured onto the reconfigurable array.

100. (New) The data processing method of claim 99, wherein the explicitly software managed cache is preloadable via a burst-preload instruction triggered by the at least one standard processor.

101. (New) The data processing method of claim 92, wherein the at least one standard processor is a RISC processor.

102. (New) The data processing method of claim 92, wherein the explicitly software managed cache is written back to the memory via a synchronization instruction.

103. (New) The data processing method of claim 92, wherein the cache is used to eliminate at least some explicit store instructions using cache-back operations.

104. (New) The data processing method of claim 103, wherein store is executed delayed as cache write back.

105. (New) The data processing method of claim 92, wherein the reconfigurable array supports pipeline stages of Load, Execute, and Store.

106. (New) The data processing method of claim 105, wherein the Store pipeline stage is executed as a cache write-back operation.

107. (New) A data processing method, comprising:

providing a reconfigurable array of data processing cells for data processing;

providing at least one standard processor for processing data in a sequential manner, the at least one standard processor including an instruction pipeline via which the reconfigurable array is coupled to the at least one standard processor; and

coupling the reconfigurable array to a de-centralized explicitly preloaded configuration cache, wherein the cache is adapted for being fed instructions for the reconfigurable array by the at least one standard processor.

108. (New) The data processing method of claim 107, wherein the data processing cells are coarse-grained cells.

109. (New) The data processing method of claim 107, wherein the reconfigurable array is runtime reconfigurable.

110. (New) The data processing method of claim 107, wherein the reconfigurable array is an FPGA.

111. (New) The data processing method of claim 107, wherein the reconfigurable array is a DSP.

112. (New) The data processing method of claim 107, wherein the reconfigurable array is a data-flow-processor.

113. (New) The data processing method of claim 107, wherein the non-preemptive configurations are executed on the reconfigurable array.

114. (New) The data processing method of claim 107, wherein the cache is used for supporting preloading of at least one configuration.

115. (New) The data processing method of claim 107, wherein the cache is used for supporting preloading of several configurations.

116. (New) The data processing method of claim 107, wherein the cache is used for supporting preloading of a fast configuration switch.

117. (New) The data processing method of claim 107, wherein the cache is used for supporting preloading of several configurations and a fast configuration switch.

118. (New) The data processing method of claim 107, wherein the cache is a FIFO.

119. (New) The data processing method of claim 107, wherein the reconfigurable processor operates asynchronously to the at least one standard processor.

120. (New) The data processing method of claim 107, wherein the reconfigurable processor and the at least one standard processor are synchronized via at least one explicit instruction.

121. (New) A data processing method, comprising:

providing a reconfigurable array of data processing cells for data processing;

providing at least one standard processor for processing data in a sequential manner, the at least one standard processor including an instruction pipeline via which the reconfigurable array is coupled to the at least one standard processor;

coupling the reconfigurable array to a cache for data processing, the cache containing local cache copies of a main memory, including a plurality of IRAM memory elements, and being explicitly software managed; and

coupling the reconfigurable array to a de-centralized explicitly preloaded configuration cache, thereby supporting preloading of at least one of a configuration and a fast configuration switch.

122. (New) The data processing method of claim 121, wherein the data processing cells are coarse-grained cells.

123. (New) The data processing method of claim 122, wherein the reconfigurable array is runtime reconfigurable.

124. (New) The data processing method of either of claims 122 and 123, wherein the reconfigurable array is an FPGA.

125. (New) The data processing method of either of claims 122 and 123, wherein the reconfigurable array is a DSP.

126. (New) The data processing method of either of claims 122 and 123, wherein the reconfigurable array is a data-flow-processor.

127. (New) The data processing method of claim 121, wherein configurations executed on the reconfigurable array are not pre-emptive.

128. (New) The data processing method of claim 121, wherein the cache containing local cache copies of a main memory eliminates explicit store instructions using cache write-back operations.

129. (New) The data processing method of claim 128, wherein store is executed delayed as cache write back.

130. (New) The data processing method of claim 128, wherein the reconfigurable array supports pipeline stages of Load, Execute, and Store.

131. (New) The data processing method of claim 130, wherein the Store pipeline stage is executed as a cache write-back operation.

132. (New) The data processing method of claim 128, wherein the de-centralized explicitly preloaded configuration cache supports preloading of at least one of a configuration and a fast configuration switch.

133. (New) The data processing system of claim 128, wherein the de-centralized explicitly preloaded configuration cache is implemented as FIFO.

134. (New) The data processing method of claim 128, wherein the reconfigurable array operates asynchronously to the at least one standard processor.

135. (New) The data processing method of claim 128, wherein the reconfigurable array and the at least one standard processor are synchronized via at least one explicit instruction.